Background section of the present application at page 2, line 20 to page 3, line 5: "[m]ultiplexors are known in the art and use control signals to shift input data among output lines based upon the control signals. Multiplexors can require many inputs for the data lines and the control signals, and each data input can require a separate data line and individual transistor for interfacing the data line with a corresponding logic gate that performs the data shifting. Due to the high number of inputs, individual data lines increase the number of transistors required for each gate, thus increasing the area and power consumption of each gate."

The logic circuit for use in a multiplexer as recited in claim 1 solves the problem noted above by using data sharing among field-effect transistors (FETs) in order to reduce the number of transistors required by each logic gate. Therefore, instead of using a separate transistor for each input data line to each logic gate, only a single transistor is required in this example for a particular data input. The other data inputs are received from adjacent or other logic gates using shared data lines. (See page 4, lines 12-16 of the specification.) Referring to Figure 2A of the present application, a single transistor 40 is required for data input DATL on logic gate 11, for example. The data sharing on lines 61-64 provides for the elimination of additional transistors. "In particular, if logic gate 11 did not have data sharing , it would typically require an additional transistor for each of the data inputs on lines 61-64. Those transistors, if used, would interface the individual data lines with logic gate 11 in the same manner as transistor 40 interfacing data line 15 with logic gate 11. Elimination of those transistors results in a savings of area and power consumption." (See page 7, lines 9-14.)

Tanihira certainly does not disclose or suggest this feature of using a single transistor for each data input in order to reduce the number of transistors required by each logic gate. Even if Tanihira's input goes though a transistor, as asserted by the Examiner, Tanihira does not disclose or teach "each of the logic gates receives one data input using the single transistor for the data input and receives other data inputs from the plurality of shared data lines" as recited in claim 1. Since Tanihira does not disclose or suggest all of the elements of claim 1, claim 1 is allowable over Tanihira.

Claims 2-10 are allowable because they depend from allowable claim 1 and for the additional features they recite.

For the same reason as discussed above with respect to claim 1, Tanihira does not disclose or suggest "wherein each data input uses a single transistor; ... wherein the plurality of shared data lines interface through a transistor on each of the logic gates to provide a portion of the data inputs for each of the logic gates by connecting data inputs among the

plurality of logic gates; ... wherein each of the logic gates receives one data input using the single transistor for the data input and receives other data inputs from the plurality of shared data lines" as recited in claim 11. Since Tanihira does not disclose or suggest all of the elements of claim 11, claim 11 is allowable over Tanihira.

Claims 12-20 are allowable because they depend from allowable claim 11 and for the additional features they recite. Withdrawal of the rejection of claims 1-20 under 35 U.S.C. §102 (b) is respectfully requested.

Claim Rejections Under 35 U.S.C. §103

Claims 8 and 18 are rejected under 35 U.S.C. §103 (a) over Tanihira in view of U.S. Patent 5,822,231 to Wong et al. (hereafter Wong). This rejection is respectfully traversed.

Claims 8 and 18 are allowable because they depend from allowable claims 1 and 11, respectively, and for the additional features they recite. Withdrawal of the rejection of claims 8 and 18 under 35 U.S.C. §103 (a) is respectfully requested.

In view of the above remarks, Applicant respectfully requests reconsideration and allowance of all pending claims.

Respectfully Submitted,

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